FE1.1s – *Revision B*

USB 2.0 High Speed 4-Port Hub Controller

Data Sheet

Introduction

The FE1.1s is a highly integrated, high quality, high performance, low power consumption, yet low cost solution for USB 4-Port Hub. It is fully compliant to "*Universal Serial Bus Specification Revision 2.0*", and supports USB-IF "*Battery Charging Specification Revision 1.1*".

It adopts *Single Transaction Translator* (STT) architecture to be more cost effective. Six, instead of two, non-periodic transaction buffers are used to minimize potential traffic jamming. The whole design is based on state-machine-control to reduce the response delay time; no micro controller is used in this chip.

To guarantee high quality, the whole chip is covered by *Test Scan Chain* – even on the high speed (480MHz) modules, so that all the logic components could be fully tested before shipping. Special *Build-In-Self-Test* mode is designed to exercise all high, full, and low speed Analog Front End (AFE) components on the packaging and testing stages as well.

Low power consumption is achieved by using advanced technology and comprehensive power/clock control mechanism.

FE1.1s could be optionally configured to support *Charging Downstream Ports* as defined by the USB-IF Battery Charging Specification. With this feature enabled, an USB hub could be easily transformed into a charging station for battery based portable devices.

Features

- Fully compliant with Universal Serial Bus Specification Revision 2.0 (USB 2.0);
  - Upstream facing port supports High-Speed (480MHz) and Full-Speed (12MHz) modes;
  - 4 downstream facing ports support High-Speed (480MHz), Full-Speed (12MHz), and Low-Speed (1.5MHz) modes;
- Integrated USB 2.0 Transceivers;
- Integrated upstream 1.5KΩ pull-up, downstream 15KΩ pull-down, and serial resisters;
- Integrated 5V to 3.3V and 1.8V regulator.
- Integrated Power-On-Reset circuit;
- Integrated 12MHz Oscillator with feedback resister, and crystal load capacitance;
- Integrated 12MHz-to-480MHz Phase Lock Loop (PLL);

- *Single Transaction Translator* (STT) –
  - One TT for all downstream ports;
  - The TT could handle 64 periodic Start-Split transactions, 32 periodic Complete-Split transactions, and 6 none-periodic transactions;
- Automatic self-power status monitoring;
  - Automatic re-enumeration when Self-Powered switching to Bus-Powered;
- *Ganged Power Control* and *Global Over-Current Detection* support;
- EEPROM configured options –
  - *Vendor ID*, *Product ID*, & *Device Release Number*; and
  - *Number of Downstream Ports*;
- Comprehensive Port Indicators support:
  - *Downstream Port Enabled* indicator LED (x4, Green);
  - *Hub Active/Suspend* indicator LED.
- Supports charging port detection mechanism on all 4 downstream ports.

BLOCK DIAGRAM

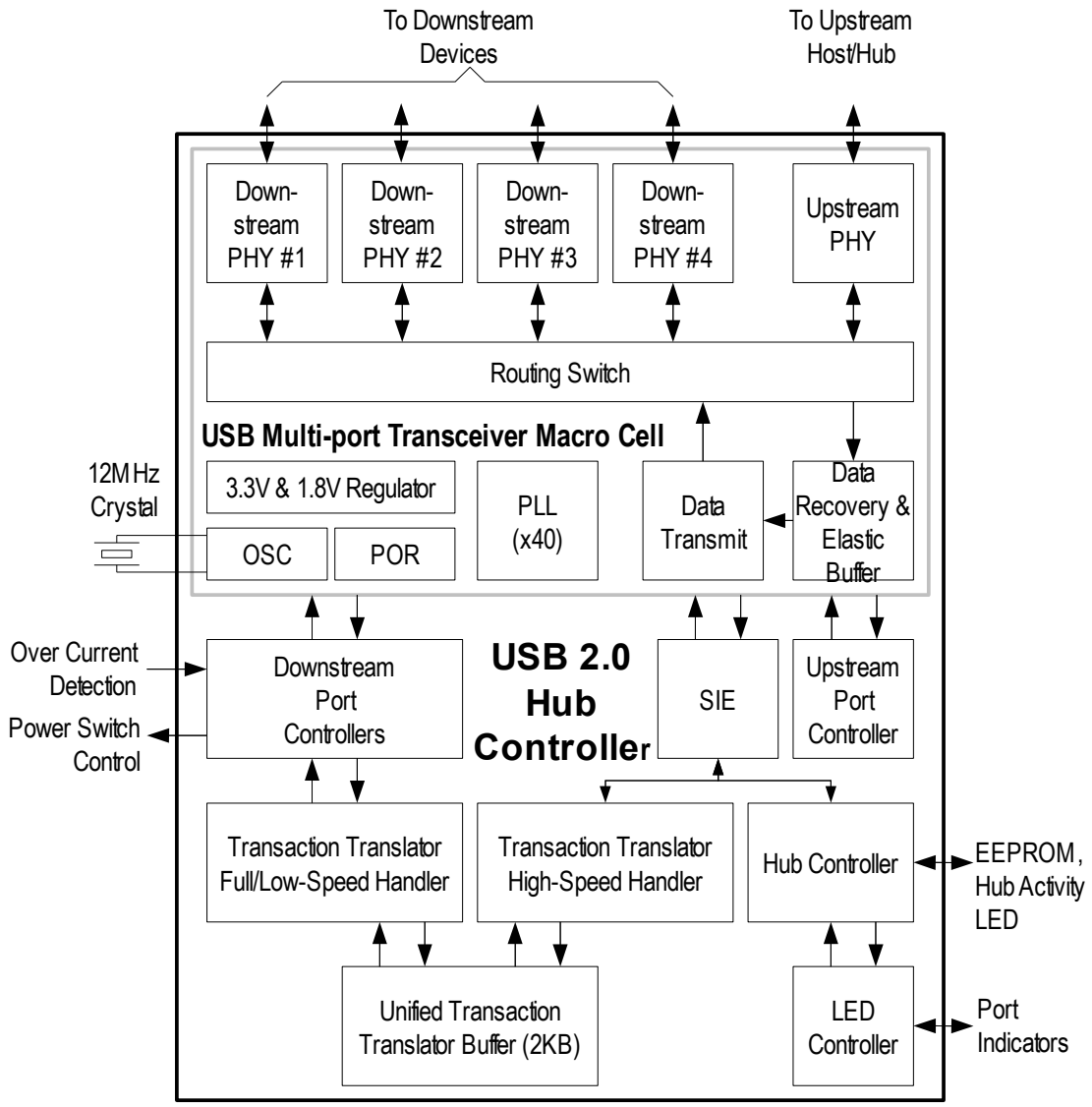


Fig. 1: Block Diagram

Package

28-pin SSOP
(Body Size: 10x4 mm, Pitch: 0.64 mm)

Pin Assignment

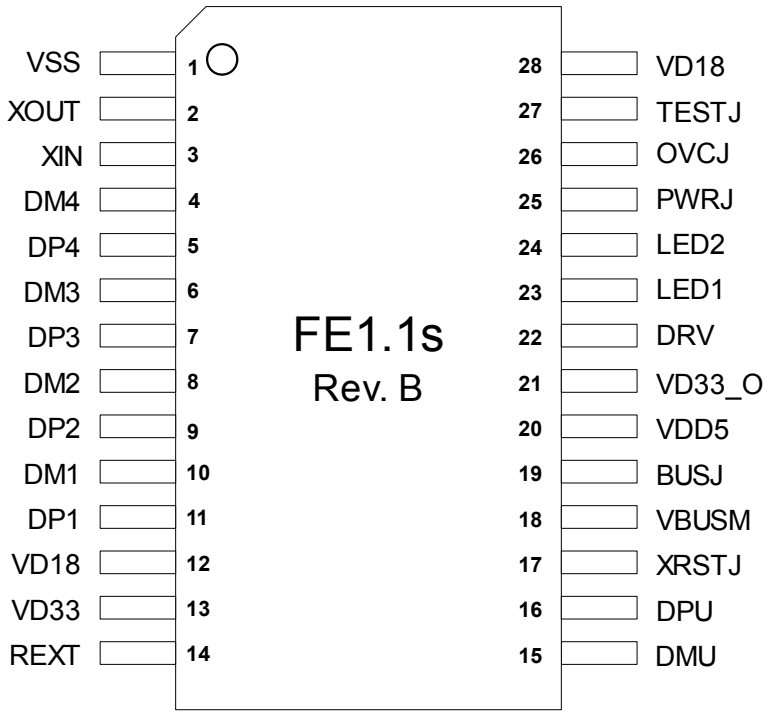


Fig. 2: SSOP-28 Pin Assignment

Pin Description Table

Pin Name	Pin No	Type	Function	Note
VSS	1	P	Ground.	
XOUT	2	OSC	12 MHz Crystal Oscillator output	1
XIN	3	OSC	12 MHz Crystal Oscillator input.	1
DM4	4	UT	The D- pin of the 4th Downstream Facing Port.	
DP4	5	UT	The D+ pin of the 4th Downstream Facing Port.	
DM3	6	UT	The D- pin of the 3rd Downstream Facing Port.	
DP3	7	UT	The D+ pin of the 3rd Downstream Facing Port.	
DM2	8	UT	The D- pin of the 2nd Downstream Facing Port.	
DP2	9	UT	The D+ pin of the 2nd Downstream Facing Port.	
DM1	10	UT	The D- pin of the 1st Downstream Facing Port.	
DP1	11	UT	The D+ pin of the 1st Downstream Facing Port.	
VD18	12, 28	P	1.8V power output	
VD33	13	P	3.3V power input for 3.3V→1.8V integrated regulator.	
REXT	14		External Bias Resisters: A 2.7KΩ (± 1%) resister should be connected to VSS to provide internal bias reference.	
DMU	15	UT	The D- pin of the Upstream Facing Port.	
DPU	16	UT	The D+ pin of the Upstream Facing Port.	
XRSTJ	17	I	External Reset: active low, is an optional source of chip reset signal. The minimum low pulse width is 10 µs. In normal applications, there is no need for this signal, and should be tied to high.	
VBUSM	18	I	Upstream Port Power Monitor: This pin monitors the power state of V_{BUS} from upstream facing port. High level indicates that the host is powered up and the hub should function normally. Low level indicates that the host is powered down, and the hub should be in power-down state.	
BUSJ	19	I	Bus Power Sense: This pin identify the primary power source of the hub. High level indicates the hub is *Self-Powered* and has enough strength to support High-Power devices on its downstream ports. Otherwise, it is *Bus-Powered* and each downstream ports are presumed to supply 100mA of power only.	
VDD5	20	P	5V power input for integrated 5V→3.3V regulator.	
VD33_O	21	P	3.3V power output from 5V→3.3V integrated regulator – a 10µF decoupling capacitor is required.	

DRV/ CHRGEN	22	I/O	LED Drive Control/Charging Hub Enable During power-on-reset, this pin is used as Charging Hub Enable. If it is tied to high, the battery charging function will be enabled. Otherwise, it is a normal hub and this pin functions as LED driving control pin.	
LED1/ EESCL	23	I/O	LED Control 1/External EEPROM Clock Port 1 and Port 3 device connected indicator (LED) control; or, when LED2 is tied to high during power-on-reset, it is the joint indicator for all ports. At the same time, it could also be used as the clock (SCL) of external EEPROM.	
LED2/ JLEDEN	24	I/O	LED Control 2/Joint LED Indicator Enable Port 2 and Port 4 device connected indicator (LED) control. During power-on-reset, it is a configuration input for enabling Joint Port Indicator by tying to 3.3V.	
PWRJ	25	OD	Power Enable This is an active low, open-drain output signal for controlling power to the downstream devices in *Ganged Power Switching* mode. It is enabled and disabled by the host hub driver to reduce the in-rush current or in response to Over-Current Detection.	
OVCJ	26	I	Over Current Sense Active low input from external current monitor indicating over-current condition for *Global Over-Current Protection.*	
TESTJ/ EESDA	27	OD-PU	Test Mode Enable/External EEPROM Serial Data Active low, open drain signal with internal pull-up resistor. When tied to low during power-on-reset, the chip will be set in test mode. The test mode is for factory test only, for all applications, this pin should be either left as *No-Connection* or connected to the Serial Data/Address (SDA) pin of external 2-wire EEPROM.	

Type Abbreviation –

I : Schmitt Trigger Input, 3.3V 5V-Tolerant;

O: Output (driving strength: 8mA);

OD: Output, Open Drain (sink current: 4 mA);

OD-PU: 3.3V Input/Output, Open Drain with Internal Pull-Up (sink current: 4 mA)

I-PU: 3.3V Input with Internal Pull-Up;

UTD: USB Downstream Facing Port Transceiver (supporting High/Full/Low Speed).

UTU: USB Upstream Facing Port Transceiver (supporting High/Full Speed).

OSC: Crystal Oscillator (with integrated feedback resister, and crystal load capacitor).

P: Power/Ground.

Note 1 – Crystal Requirements

- Frequency accuracy: 12MHz ± 50ppm
- Load capacitance: 16pF ~ 20pF

Application Alternatives

The *FE1.1s* can be configured through board design options in one of three modes – *Individual Port Active Indicator* mode, *Joint Port Active Indicator* mode, and *USB Battery Charging Hub* more. Each mode could incorporate an optional external serial EEPROM for customizing *Vendor ID*, *Product ID*, *Device Release Number*, and number of ports. The detailed layout of EEPROM contents is explained in the following section.

All these options are implemented through four pins of FE1.1s: DRV, LED1, LED2, and TEST.

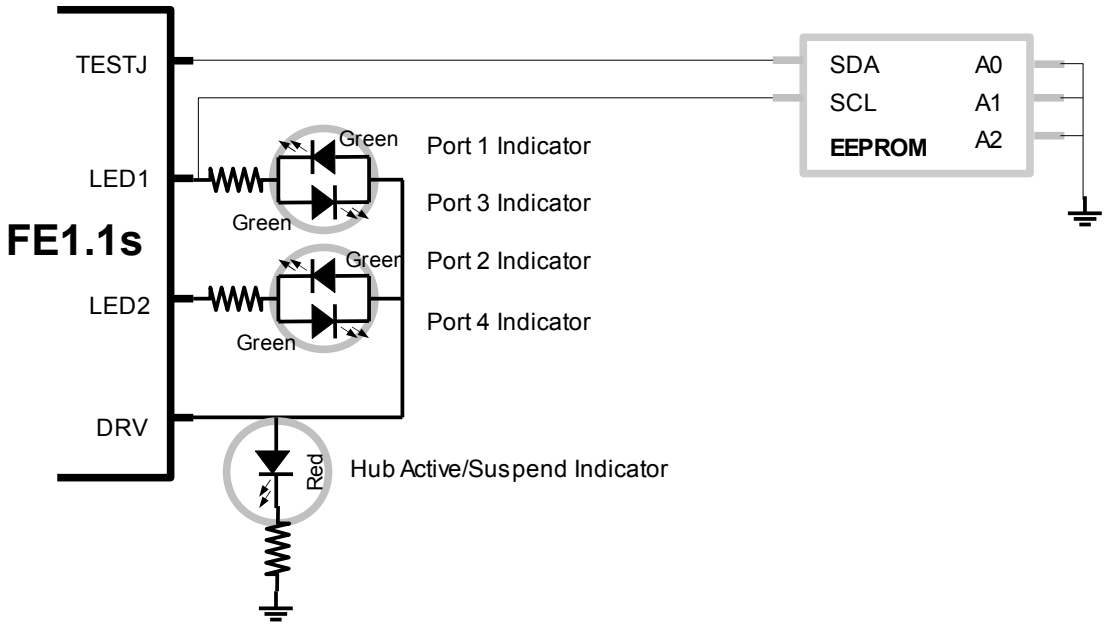


Fig. 3: LED and EEPROM Connections

Individual Port Active Indicator Mode

In this mode, as shown by Fig. 3, FE1.1s supports up to 5 LED's. There is one green LED for each downstream port and one red LED for hub active/suspend indication. The green light turns on whenever a device properly attached to its corresponding port, and turns off when it is disconnected or the bus is suspended. The red light turns on when the hub is configured by the USB host, and turns off when it is detached from the host or switch into suspend mode. All LED's are optional and could be safely omitted without any special measures. The external serial EEPROM is optionally hooked on TESTJ and LED1.

Joint Port Active Indicator Mode

The four downstream port active indicators can be joint into one single LED, as depicted in Fig. 4, by tying LED2 to 3.3V. In this mode, the Joint Port Indicator will turn on whenever there is at least one device attached to any one of the four downstream ports. The behavior of the Hub Active/Suspend Indicator and the external serial EEPROM are remained unchanged.

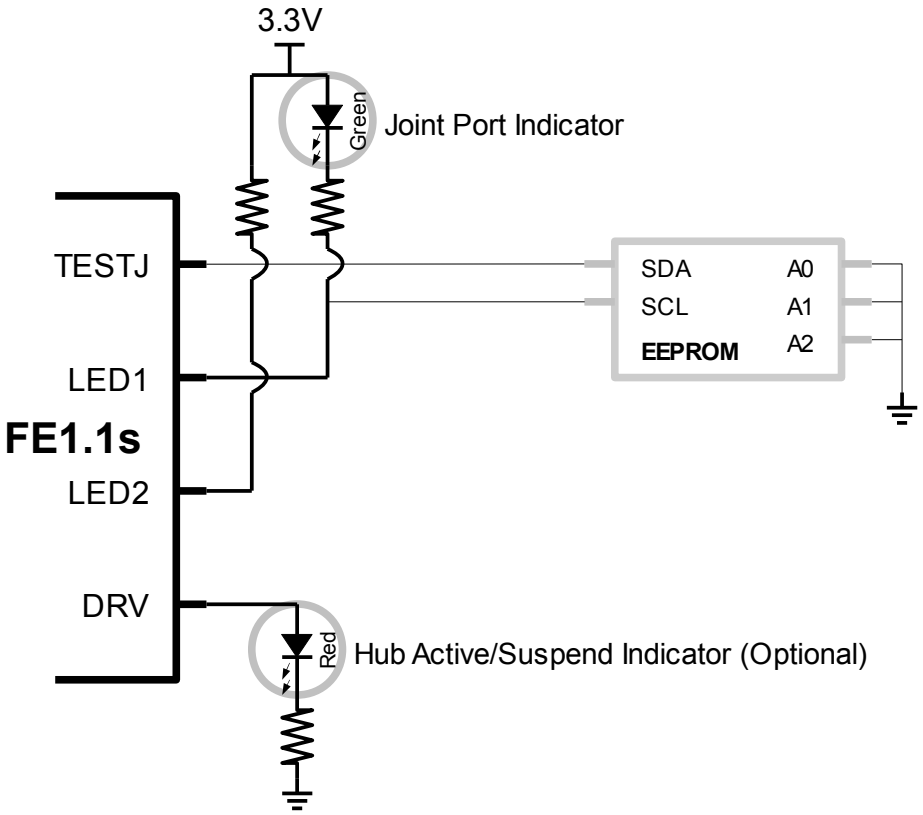


Fig. 4: Joint Port Active Indicator

USB Battery Charging Hub

The FE1.1s Revision B could be optionally configured to support USB Battery Charging Specification 1.1 and provides the core control logic for USB Charging Hub. In this mode, the hub will be ready to respond to the charging request from portable devices no matter whether it is not connected to the host, the host being powered down, in normal operation, or in suspend. In other words, as long as the hub itself is properly powered, the charging function is independent of the status of the upstream port or the host controller.

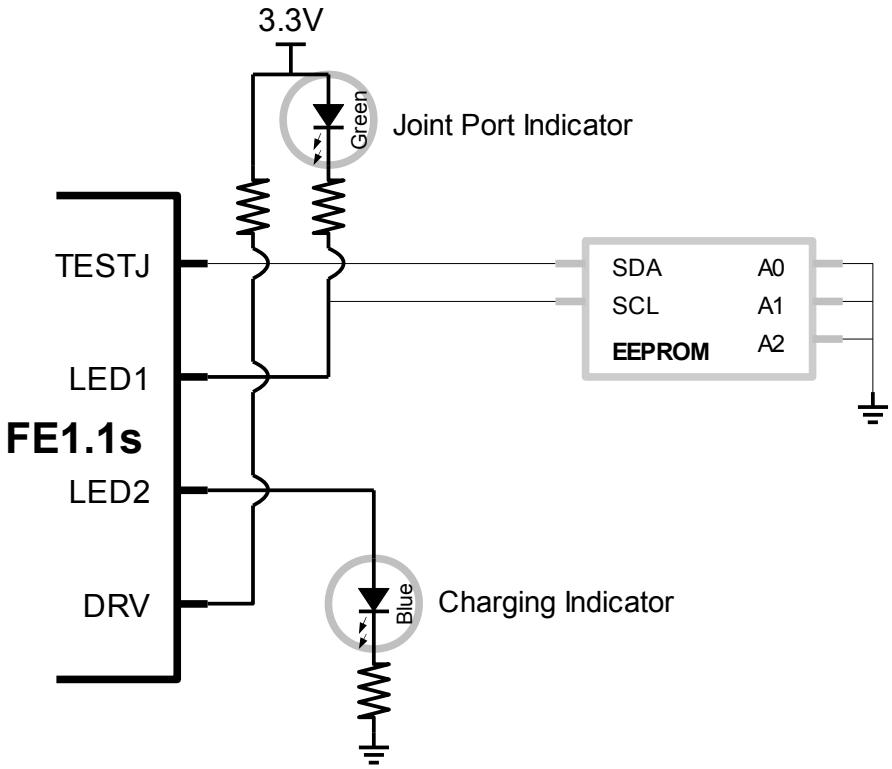


Fig. 5: USB Charging Hub

Figure 4 demonstrates this configuration. The DRV pin is tied to 3.3V to set FE1.1 into USB Charging Hub mode. The LED2 will then be the Charging Indicator which turns on the LED when a successful charging request handshake between the hub and the portable device completed. The LED1 is the Joint Port Indicator which turns on the LED when at least one device connected successfully on any of the downstream ports. An external Serial EEPROM could be optionally hooked on LED1 and TESTJ to provide alternate PID, VID, etc.

EEPROM Contents

Address	Contents	Note
0x00	0x40	Constant, low byte of check code
0x01	0x1A	Constant, high byte of check code
0x02	Vendor ID (Low)	Low byte of Vendor ID, idVendor field of *Standard Device Descriptor*
0x03	Vendor ID (High)	High byte of Vendor ID
0x04	Product ID (Low)	Low byte of Product ID, idProduct field of *Standard Device Descriptor*
0x05	Product ID (High)	High Byte of Product ID
0x06	Device Release (Low)	Low byte of Device Release Number, must be Binary Coded Decimal, bcdDevice field of *Standard Device Descriptor*
0x07	Device Release (High)	High byte of Device Release Number, must be Binary Coded Decimal
0x08 ~ 0x19	Filling	All 0x00
0x1A	Port Number	Number of Downstream Ports, bNbrPorts field of *Hub Descriptor.*
0x1B ~ 0x1E	Filling	All 0x00
0x1F	Check Sum	The 8-bit sum of all value from 0x00 to 0x1E.

The first two bytes are the check code from the existence of EEPROM, their value must be 0x1A40. Any other value would cause the EEPROM loading mechanism of *FE1.1s* to conclude that the contents of this EEPROM is unusable, and use the default value instead.

The last byte, 0x1F, is a checksum made up of the sum of all value from 0x00 to 0x1E. The number must match to render the content of the EEPROM usable. Otherwise, the loading mechanism of *FE1.1s* would discard the value from EEPROM and use default value instead.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	TS	-55	+150	℃
Power Supply Voltage	VDD5 VD33	-0.5 -0.5	+6.0 +4.0	V
ESD Human Body Mode		-2000	2000	V
ESD Machine Mode		-200	200	V
ESD Charged Device Mode		-500	500	V
Latch Up		-200	200	mA

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	TA	0		70	℃
Operating voltage	VDD5 VD33	4.5 3.0	5.0 3.3	5.5 3.6	V
LOW level voltage of digital input	VIL	-0.3		0.8	V
HIGH level voltage of digital input	VIH	2.0		5.5	V
Threshold voltage of digital input	VTH	1.45	1.58	1.74	V
Low-to-High level of schmitt-trigger input	VT+	1.44	1.5	1.56	V
High-to-Low level of schmitt-trigger input	VT-	0.89	0.94	0.99	V
LOW level voltage of digital output@4mA	VOL			0.4	V
HIGH level voltage of digital output@4mA	VOH	2.4			V
XIN input capacitance	Cin		32		pF
Internal Pull-Up Resister Range	R_{PU}	39	65	116	KΩ

POWER CONSUMPTION

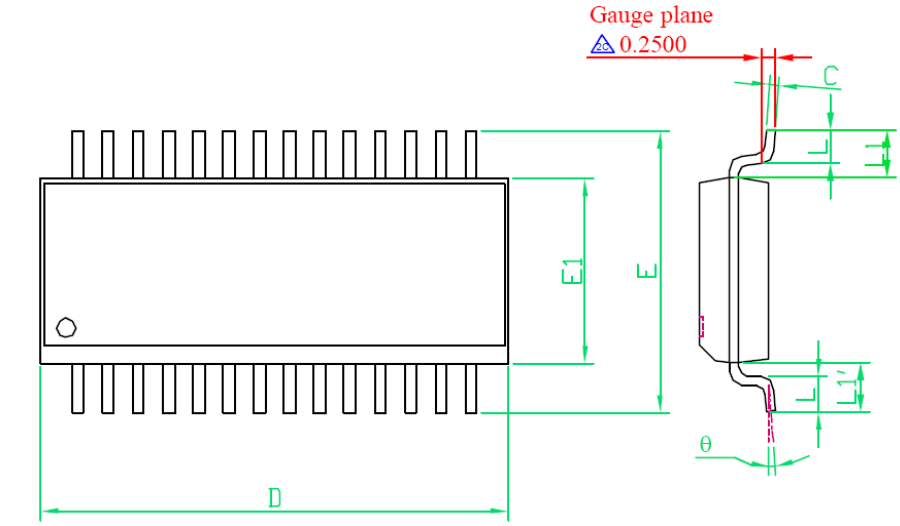
DC SUPPLY CURRENT

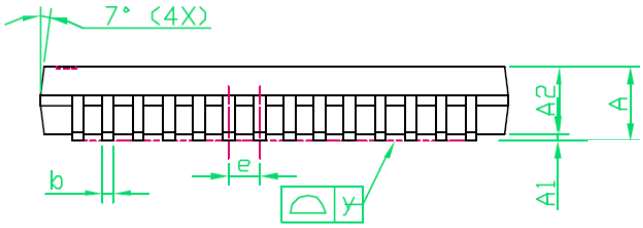
Symbol	Condition			Typ.	Unit
	Active ports	Host	Device		
I_suspend	Suspend			800	uA
I_suspend_cm	Suspend in Charging Mode			1300	uA
Icc	4	Full-Speed	4x Full-Speed	28	mA
		High-Speed	4x High-Speed	84	mA
		High-Speed	4x Full-Speed	41	mA
	3	Full-Speed	3x Full-Speed	28	mA
		High-Speed	3x High-Speed	73	mA
		High-Speed	3x Full-Speed	41	mA
	2	Full-Speed	2x Full-Speed	28	mA
		High-Speed	2x High-Speed	62	mA
		High-Speed	2x Full-Speed	41	mA
	1	Full-Speed	1x Full-Speed	28	mA
		High-Speed	1x High-Speed	51	mA
		High-Speed	1x Full-Speed	41	mA
	No active	Full-Speed		28	mA
		High-Speed		40	mA

Note: The power consumption is measured when the bus is in IDLE state – there is no activities other than the Start-Of-Frame (SOF) and INTERRUPT-IN packets for the hub itself on the bus. The peak power consumption varies depending upon the system configuration, type of operations, and over-all bus utilization.

PACKAGE

28-pin SSOP (Body Size: 10x4 mm, Pitch: 0.64mm)





SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.60	1.75	0.053	0.064	0.069
A1	0.10	---	0.25	0.004	---	0.010
A2	---	1.45	---	---	0.057	---
b	0.20	0.25	0.30	0.008	0.010	0.012
C	0.19	---	0.25	0.007	---	0.010
D	9.80	---	10.00	0.386	---	0.394
E	5.80	6.0	6.20	0.228	0.236	0.244
E1	3.80	3.9	4.00	0.150	0.153	0.157
e	---	0.64	---	---	0.025	---
L	0.40	---	1.27	0.016	---	0.050
y	---	---	0.10	---	---	0.004
θ	0°	---	8°	0°	---	8°
L1-L1'	---	---	0.12	---	---	0.005
L1	1.04REF			0.041REF		

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